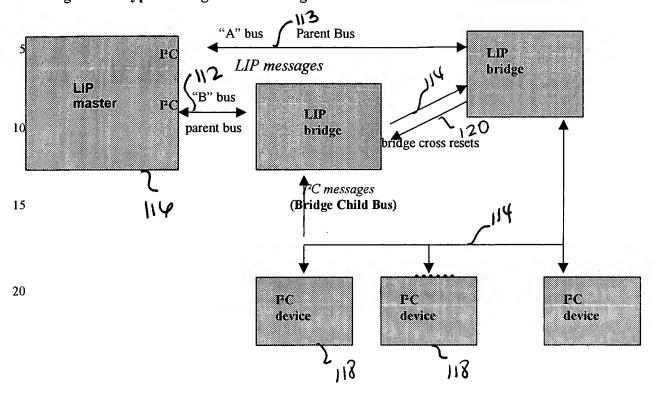


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Figure 3: Typical Usage of LIP Bridge



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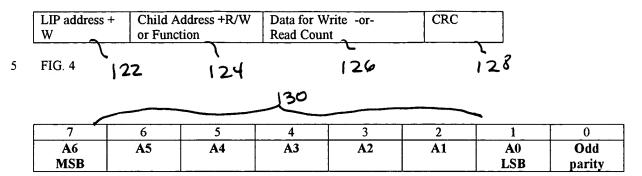


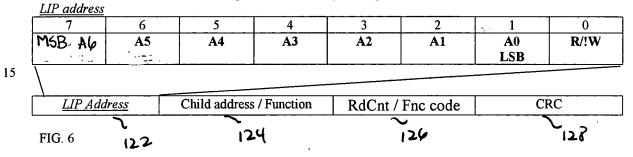
FIG. 5

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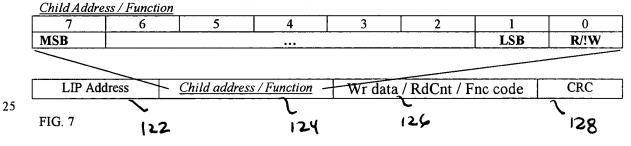
20

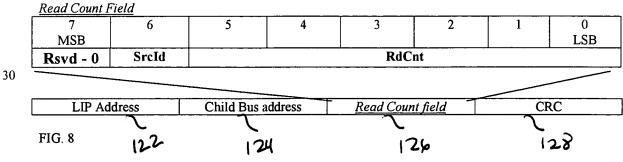
Hardware Address Strapping

The LIP Address / Function encoding within the four byte LIP packet is as follows:

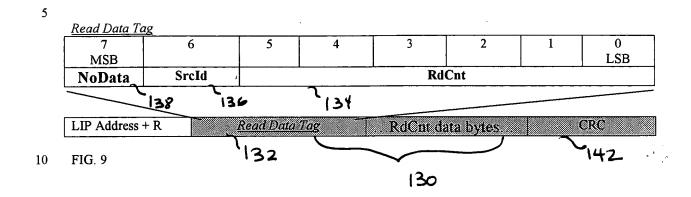


The Child Address / Function encoding is as follows:





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15 Status Byte Register Organization

RAZ	RAZ	RAZ	ME	LBWE	LBRE	CBWE	CBRE
MSB							LSB
FIG. 10							
			•	, EO			Fig. 1
				150			•

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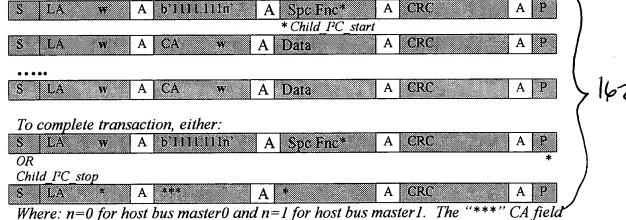
Table 8	3
Key to	Symbols

Symbol	Meaning
S	I ² C bus start condition
P	I ² C bus stop condition
Α	Acknowledge
Α	No-Acknowledge
LA	LIP address
CA	Child bus address
\mathbf{W}	R/!W bit within address field is set for WRITE
R	R/!W bit within address field is set for READ
CRC	CRC byte
Data	Data byte
Count	Read count
Fnc(x)	Special function command "x" – where x is the function's hex code
	Gray shade indicates data sent from host bus master to LIP bridge
	White indicates data sent from LIP bridge to host bus master
••••	Zero or more instances of the preceding transaction.

5 Host bus master to LIP One Byte Child Bus Write
S LA w A CA w A Data A CRC A P

FIG. 11

Host bus master to LIP Multi-Byte Write



contains a different value than that contained in the first data packet (SECOND PACKET ABOVE). This can be either a different child address, or it can be a special function indicator of binary '1111.111n'.

FIG. 12



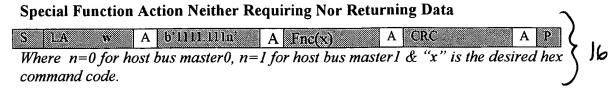
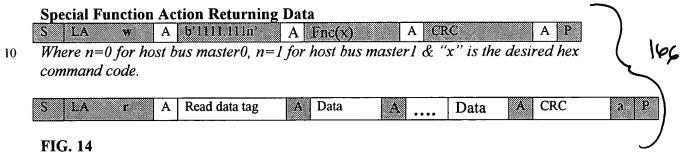
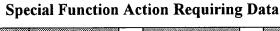


FIG. 13

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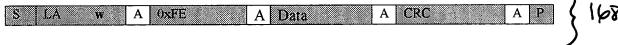


FIG. 15

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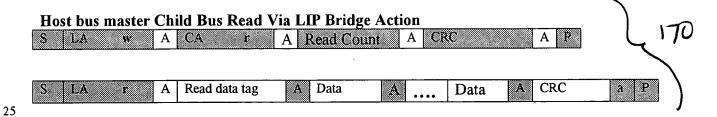
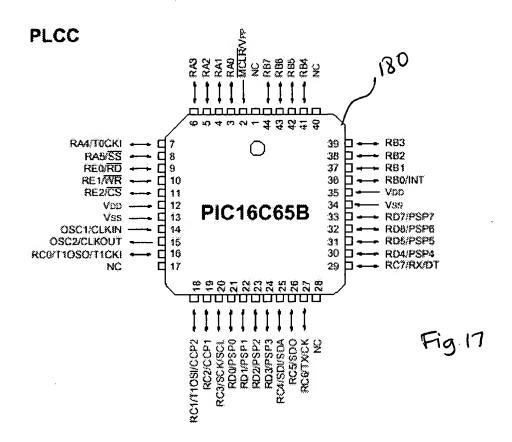
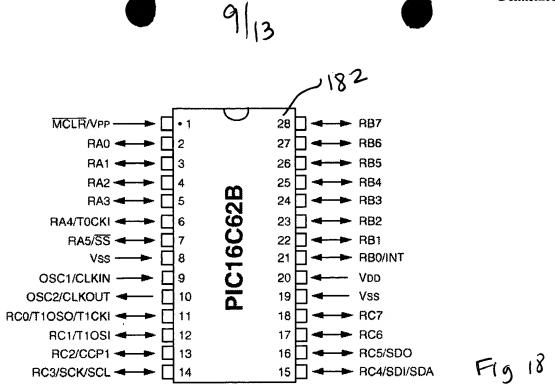


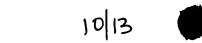
FIG. 16



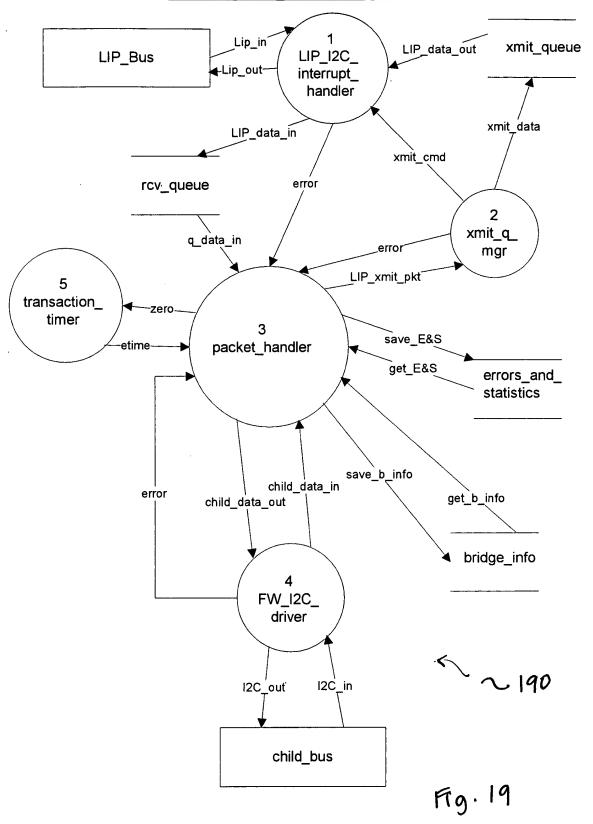
PIN#	Label	Function	
2	!MCLR	!partner_reset_in Active low input for reset from partner LIP bridge	
_		(Also VPP pin for in circuit programming)	
3	RA0	!partner reset out – Active low output to reset partner LIP bridge	
20	RC3	LIP clk LIP bus serial clock in	
25	RC4	LIP_data LIP bus serial data in/out (bidirectional)	
27	RC6	Child_clk child bus clock output	
29	RC7	Child_data - child bus data in/out (bidirectional)	
37	RB1	LIP_addr_parity - parity bit for LIP address (strap to make odd parity)	
38	RB2	LIP_addr0 - bit 0 to strap LIP I ² C address	
39	RB3	LIP_addr1 - bit 1 to strap LIP I ² C address	
41	RB4	LIP_addr2 – bit 2 to strap LIP I ² C address	
42	RB5	LIP addr3 – bit 3 to strap LIP I ² C address	
4	RA1	LIP_addr4 - bit 4 to strap LIP I ² C address	
5	RA2	LIP addr5 - bit 5 to strap LIP I ² C address	
43	RB6	In circuit programming clock	
44	RB7	In circuit programming data	
6	RA3	Child bus busy_out -active low open collector output when this LIP bridge owns child bus	
		(needs a 1K pull up to Vdd).	
36	RB0	Child_bus_busy_in -active low input when partner LIP bridge owns child bus	

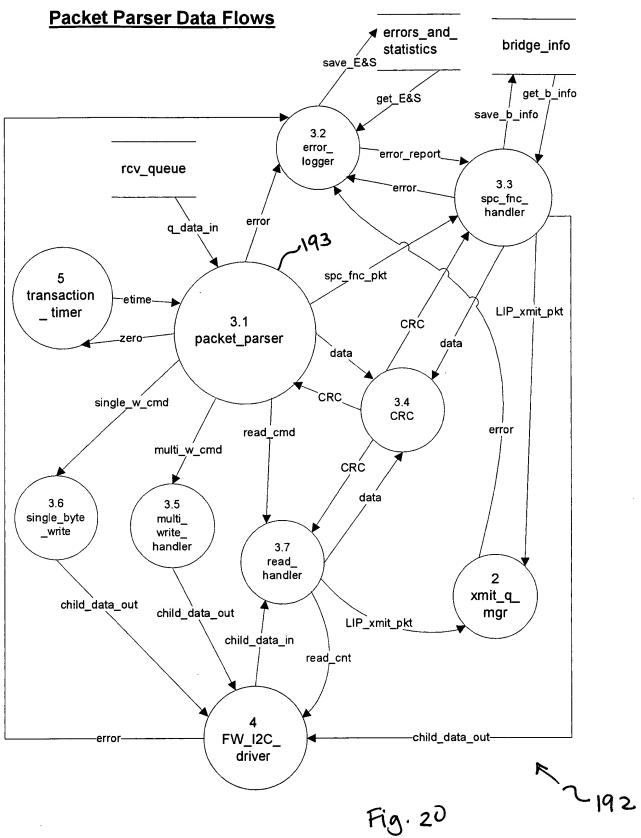


PIN#	<u>Label</u>	<u>Function</u>	
1	!MCLR	!partner_reset_in Active low input for reset from partner LIP bridge	
		(Also VPP pin for in circuit programming)	
2	RA0	!partner_reset_out - Active low output to reset partner LIP bridge	
14	RC3	LIP_clk LIP bus serial clock in	
15	RC4	LIP data LIP bus serial data in/out (bidirectional)	
17	RC6	child clk child bus clock output	
18	RC7	child data - child bus data in/out (bidirectional)	
22	RB1	LIP_addr_parity - parity bit for LIP address (strap to make odd parity)	
23	RB2	LIP_addr0 - bit 0 to strap LIP I ² C address	
24	RB3	LIP_addr1 – bit 1 to strap LIP I ² C address	
25	RB4	LIP_addr2 - bit 2 to strap LIP I ² C address	
26	RB5	LIP_addr3 - bit 3 to strap LIP I ² C address	
3	RA1	LIP_addr4 - bit 4 to strap LIP I ² C address	
4	RA2	LIP_addr5 - bit 5 to strap LIP I ² C address	
27	RB6	In circuit programming clock	
28	RB7	In circuit programming data	
5	RA3	child_bus_busy_out -active low output when this LIP bridge owns child bus (needs a 1K pull up to Vdd).	
21	RB0	child_bus_busy_in -active low input when partner LIP bridge owns child bus	



Level 1 Data Flow Diagram

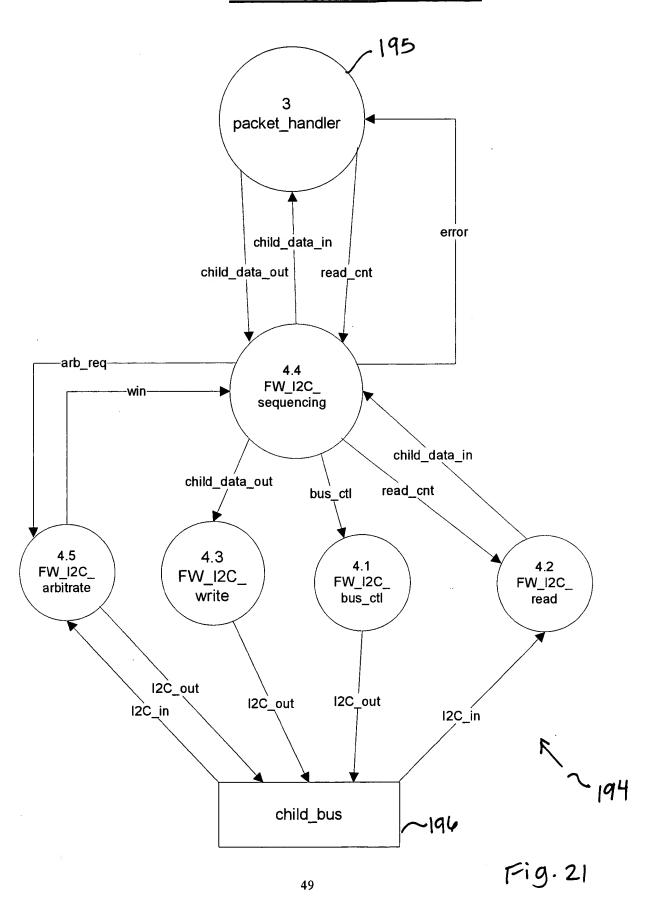




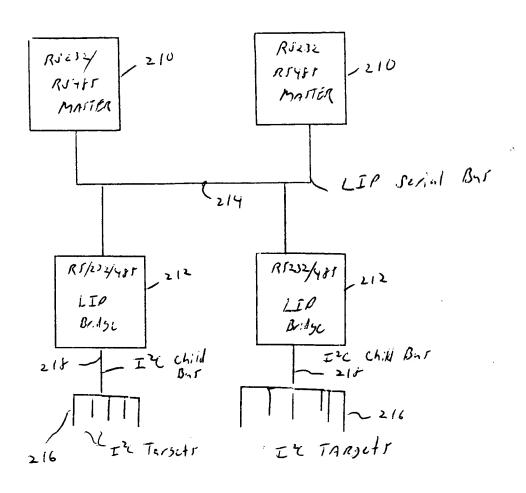




Firmware 12C Data Flows







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